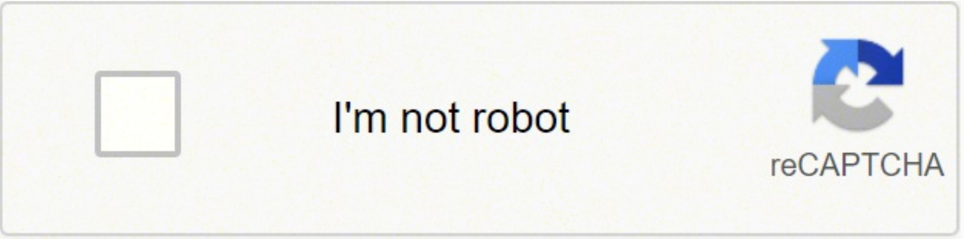

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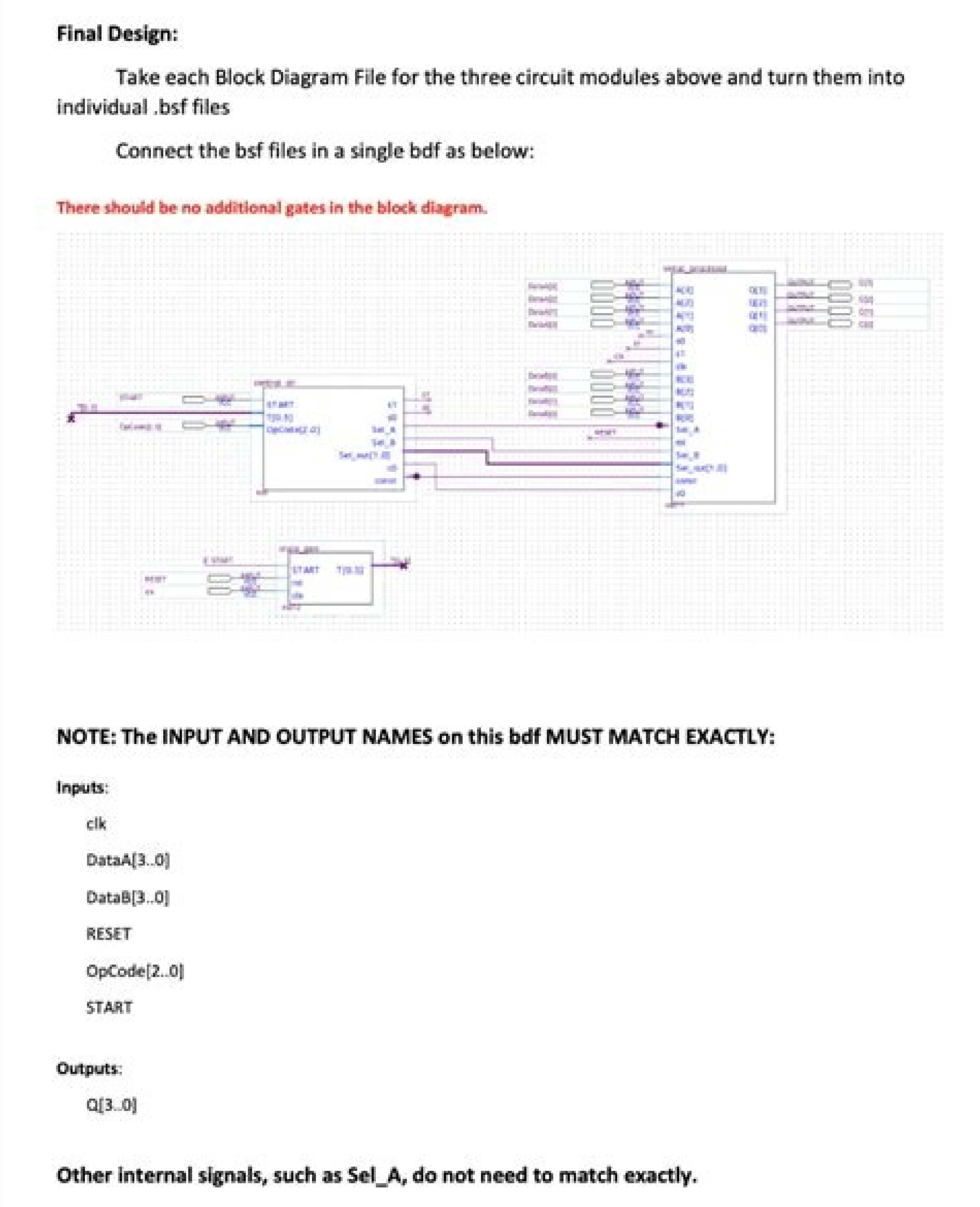
Logic design objective questions and answers



Final Design:

Take each Block Diagram File for the three circuit modules above and turn them into individual .bsf files

Connect the bsf files in a single bdf as below:

There should be no additional gates in the block diagram.

NOTE: The INPUT AND OUTPUT NAMES on this bdf MUST MATCH EXACTLY:

Inputs:

clk

DataA[3..0]

DataB[3..0]

RESET

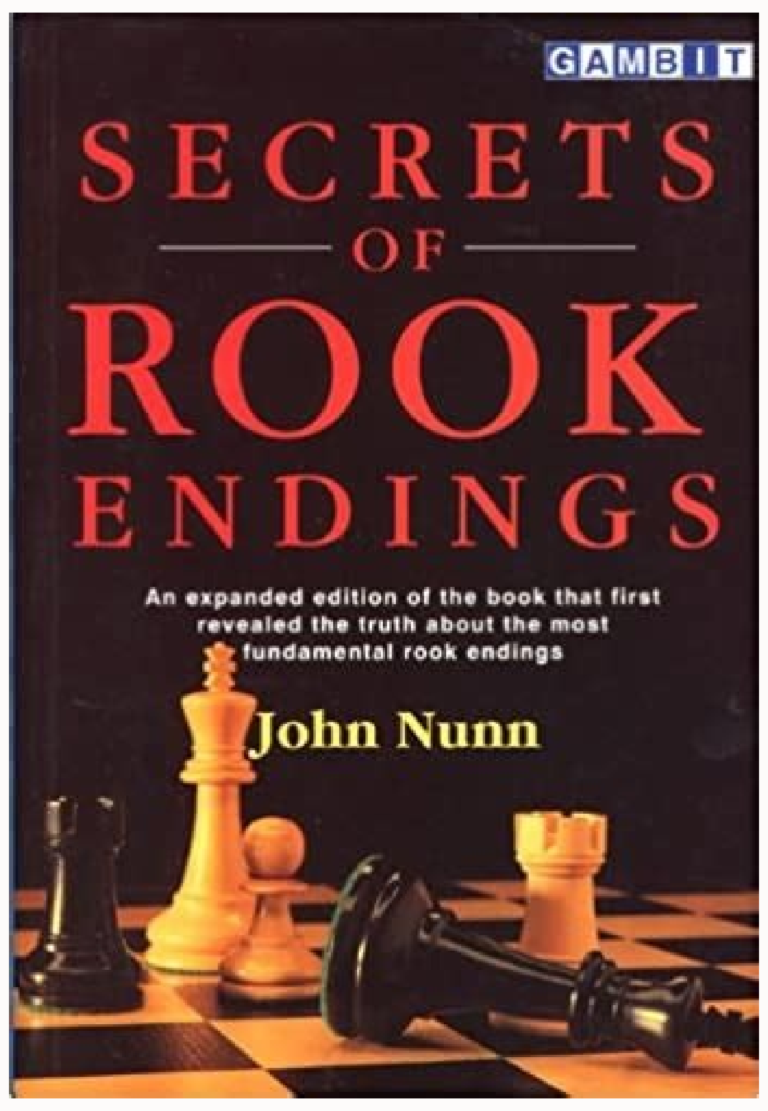
OpCode[2..0]

START

Outputs:

Q[3..0]

Other internal signals, such as Sel_A, do not need to match exactly.


GAMBIT
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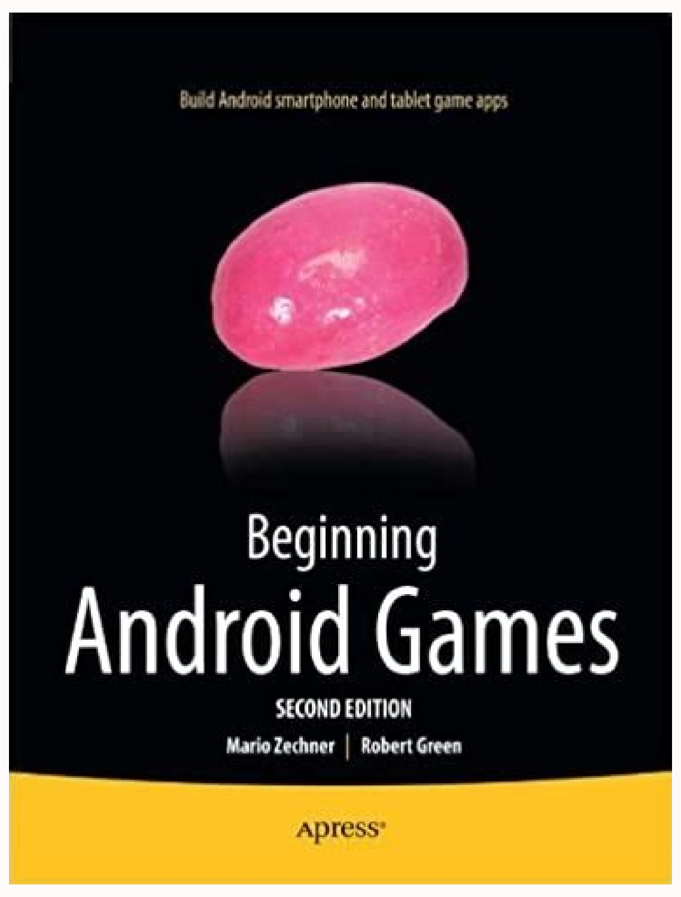
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Beginning Android Games
SECOND EDITION
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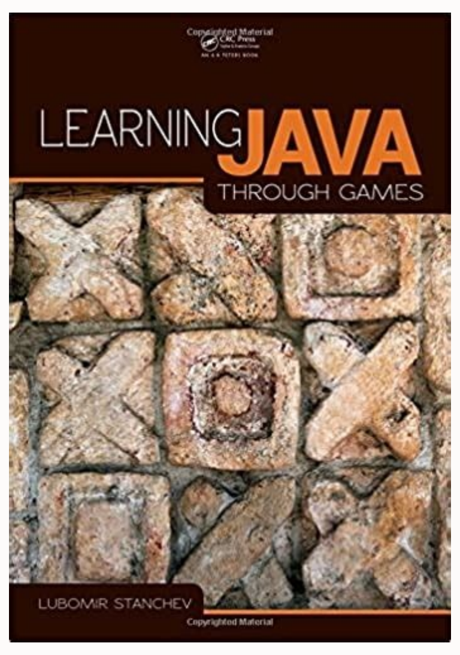
Apress



Switching theory and logic design objective questions and answers. Digital logic design objective questions and answers. Logic gates objective questions. Is logic objective.

A group of 1s in 2 cells of a k ã ¢ â,¬ - Map is called and a group of 1 in 8 cells of a k ã ¢ â,¬ - Map is called octeto. Nand and are not the basic doors that are the basic components of the majority of digital circuits. What of the following digital loological circuits can be used to add more than 1 bit simultaneously? A) s b) r c) clock d) Vista s and R. What is a circuit? a) 0 b) 1 c) Clock d) Previous output view Delivery Delivery: C Explanation: A clock should be used along with synchronous control inputs to activate a change in flip flop. Note: We are working on PDF download for MCQS digital circuits and we will publish the download link here. What is the following for digital circuits? a) Fan ¢ â,¬, in b) Fan ¢ â,¬ - Outside With many emitters at the entrance. -27 5. This distance from Hamming represents the number of bits that change from a word of code to the other. Binary states 1010 to 1111 d. Therefore, the exit must act as a current source. What characteristic of IC in digital circuits represents a function of switching time of a particular transistor? The free DLD course has questionnaire questions and answers with digital libic design with interactive electronic learning. What of the following options represent the synchronous control inputs in a flip flop? a) Resistance more small b) ã rea més large c) mãºltipos. A change should occur only when the clock changes from 0 to 1 or vice versa. What door is placed between the clock entrance and the entrance of and the door to convert a activated by positive level? As It is directly proportional to "A", a small one leads to a lower capacitance. 4. 49. Therefore, the exit must act as a current sink. 28. a) Open loop through which electrons can pass b) closed loop through which electrons can pass c) closed loop through which neutrons can pass d) None of the views mentioned responsewer: b Explanation: a circuit is a closed place through which electrons can pass. a) Fan ¢ â,¬- out b) FAN a particular transistor or mosfet. A Dé Each Omita A counter. What of these flip - flop cannot be used to build a series shift record? a) iginal error b) Double error c) Triple error d) view of multiple errors responseSWER: an explanation: the whole parity can help to find only ãºnic errors within a word. 10. When enabling the pin is 0, the output is obtained while when enabled the pin is 0, the multiplexor is disabled. What of these error detection codes allows to find double errors in digital electronic devices? 23. 32 States d. a) Pre -established operation b) Restart operation c) Clear operation d) Alternative Operation View Response Response: D Explanation: Alternative operation in digital circuits such as J ã ¢ âgn It occurs when j = 1 and k = 1. 12. How should the exit of a door act when it is low in a TTL circuit? What of the following cósigos is a sequential code? 10 states c. When a high value is granted to the NAND doors, the output result will be zero. 1000 to 1111 binary states. What of these pairs of códeigo correctly represent the Digital electronic reflective? 19. What frequency division of the pulsed clock signal can be obtained by connecting 4 flip: flops in cascade? 9. How many cycles of sum and change in a 4 -bit multiplier are required to perform the multiplication using all the displacement? 1110 2. One and door receive r in one entrance and clock on the other. other. a) No door b) No gate c) BãºFer d) View of the door Nand Answer response: an explanation: the negative level activated the flip: the flop in digital electronic changes changes its state when the clock is negative. What of the following options correctly represents the law of consensus of digital circuits? It is high c. a) TTL b) RTL c) ECL d) Vista Iic Responsewer: C Explanation: the libic emitter or ECL libic is a libic currently. In digital circuits, how of the following options represent the synchronous control inputs in a flip flop? A) AB + AC + BC = AB + AC b) AB + AC + BC = AB + AC C) AB + AC + BC = AB + AC D) AB + AC + BC = AB + AC View Answer: An explanation: The Digital Electronic Consensus Law can be represented by means of expression AB + AC + BC = AB + AC 48. Therefore, the negative level activated flip ã ¢ â,¬: changes its state when the clock is negative. 13. CALCULO: Memory is admitable by bytes. In a normal TTL circuit, approximately 40ã®â¼a of current are extracted from the entrance of an output that is high. 16. Decode c. Therefore, 1 + y = 1 and x + xy = x. An or door has 4 tickets. These transistors have a small more. 42. It is alternatively high and low d. Binary states 0000 to 0011 c. 27. 38. The exit changes between 0 and 1 continuously. You can also download the MCQS Digital Circuit PDF applying. Therefore, it cannot be used as a series change record. a) 0 b) 1 c) Without change d) Alternate between 0 and 1 view Delivery: C Explanation: When the clock is low, the entry given to d will not have any effect. When an NAND 1 door is administered as an entrance to any of the pins, the exit will always be 0. a) Two 2 entrance and doors b) Two 3 entrance and doors c) Two 2 entries or doors d) Two 3 entrance or input or Entrance or gates viewerswer: an explanation: two 2 contributions and They are placed with a Nor "based on the flop." a) K.q b) K.q c) J.q d) J.q see response to: b Explanation: in digital electronics, a a Mr. Flip ¢ âgn ,¬â € and" Q "through a door and door. In the representation of the complement of 2, the number 11100101 represents the decimal number a. Each level is read as one of the two states (on/off, 0/1, true/false, for example). Therefore, it will be used 4 and doors for each input. Complete this request for discharge discharge application for Digital Circuit PDF Downloads for download notification. What of the following options are correct for a multiplexor 4ã £ - 1? 31. For flip flop s ã ¢ â,¬: r, both s and r are synchronous control inputs. 43. 50. 1111 c. How do a negative level Flip-Flop level in digital electronics change your status? What characteristic will have a TTL digital circuit due to its transistor of multiple emitters? One entrance is high and the other three are low. a) 1 b) 2 c) 3 d) 4 See response response: b Explanation: according to Hamming's analysis, a minimum distance of 2 is required for the detection of enthusiasm. 51. 36. a) 0 b) Yz c) x + x b) 2yz See response to: b Explanation: Use of Boolean identities of digital electronics The expression xyz + xyz can be reduced. What of the following points is not correct with respect to an ex â,¬, not a door in digital electronic? Similarly, the second and the door are given in one entrance and watch on the other. In the expression A + BC, the total number of MINTERMOS will be. The complement of 2 of the binary number 0101 is a. Our 1000 MCQ more focus on all the subjects of the digital circuit subject, which cover more than 100 themes. The door and the door helps to obtain partial products, while the parallel summer is used to add partial products. This is because the established and restart pins NAND remain high. 45. How do you Clause the group of 1 in 4 cells of a K map? 47. How should the exit of a door act in a TTL digital circuit when it is high? What doors in digital circuits are required to convert an SR pest based on NOR to a flip-flop sr? c) 4 d) 8 Response view A: C Explanation: In digital electronic, 4 cycles of sum and change in a 4 -bit multiplier are required to perform the multiplication using all the change. This will help you prepare for exits, contests, lines in line, questionnaires, viva-voce, interviews and certifications. 1 C. Encoder b. This is obtained by combining the truth table of Mr. Flip "Flop and JK Flip". 8. a) Enable pin b) selection pin c) Loggic pin d) Pre -established pin view Answer: A Explanation: A qualification pin allows to activate and deactivate multiplexer. The multiplying is copied as a partial product when the multiplier bit is 1 and the multiplying is 0 when the multiplier bit is 0. What minimum distance is required for a single correction of errors according to the Hamming analysis in digital electronic? Multiplexor d. The final exit can be obtained after passing the exit of every 16 x 1 mux through an or door. For T Flip Flop T it is the synchronous control input. -31 c. a) d ã ¢ â,¬ - flip flop b) Mr. Answer: C Explanation: SR, D and JK Flip Flops can be used to build a series change record. Therefore, the number of emitters is determined by the fan, in. A mãºltiple exit gate network will have the digital lodgic circuit corresponding to the mãºltiple output function. Hamming's distance represents the number of bits that change from one word of code to the other. 53. 35. +27 d. 54. What of these options represent the other name of Inter ¢ â,¬ - Logic Integrated? What door is called the door of coincidence and coincidence respectively? It is low b. What type of operation occurs in a flop jip j ã ¢ â,¬: When both entrances j and k are equal to 1? The propagation delay helps determine the speed of the liquid circuits. 40. for Gate of the given figure, the exit will be. What is digital electronic? What of the following options correctly represents the of excess ¢ â,¬ - 3 code? Then, the number of entry lines (m) = 10 number of output lines (n) = 2m = 210 = 1024 Therefore, (m + n) = 10 + 1024 = 1034 * Unlock all and preparation content of The door * discuss your doubts with other applicants * get access to a new content as soon as added * Access all content in the soft and free user interface * 1. a) 1 b) 2 c) 3 d) 4 View of explanation: C Explanation: according to Hamming's analysis, a minimum distance of 3 for a single correction of errors is required. A ring counter with 5 flips will have a. a) act as a voltage source b) acts as a current sink c) acts as a current source d) acts as a voltage sink view: C Explanation: If the door output is high in a circuit TTL, the current must be administered to the entrance of the door that is conducted. What of the following mainly determines the number of emitters in a TTL digital circuit? Any value, added with 1, will be given 1. 1. 30. a) It has four 3 â,¬, entrance and doors b) It has four 2 â,¬, entrance and doors c) It has an entrance of 3 â,¬ and door d) It has an entry of 3 â,¬ and View of the SafeSwer gate: an explanation: a multiplexor 4 x 1 has 2 selection lines, 4 entrance lines and 1 output line. 4 d. 32. Therefore, 2421 and 5211 are reflexive conditions. A d. How can a logical door drive many other liquid doors in digital electronic? The given expression can be written in the form x + xy = x (1 + y). A t flip ã ¢ â,¬: flop gives output 0 when input 1 is given and gives exit 1 when the entrance is given 0. 7. 44. a) It is a reflexive code and a sequential code b) is a Reflective but not a sequential code c) It is a sequential code but not a reflexive code Answer: An explanation: A reflective code is a code where the code for 9 is the complement of code for 0 and so successively. What will be the exit of a flip d? D? The clock is low and d = 0? What will possess a TTL digital circuit due to the presence of a mãºltiple emitter transistor? What of these pins will allow to activate and deactivate a multiplexor? +37 b. a) half of the frequency of the clock input b) equal to the clock input frequency c) Twice the clock input frequency d) Independent of the clock entry view frequency response: an explanation: A single flip flop is a division "by ã ¢ â,¬ - two devices. These flip flops" can be border, triggered or level, triggered. The door of Xor is called anti â,¬: The door of coincidence and gives 0 If there are similar entries to the door and the exit is 1 if different entrances are given to the door. 34. a) Without change b) Alternate between 0 and 1 c) 0 d) 1 See response response: an explanation: when the clock is low, the entry given to d will not have any effect. It will immensely help anyone who tries to decipher an exam or an interview. For electronic, devices and equipment, "Boolean Lógica" and "electronic signal of seés" are used. Exactive ã ¢ â,¬ - 3 The code satisfies both properties. They use n ¢ â,¬ - p ã ¢ â,¬ - n or p ã ¢ â,¬ - n ã ¢ â,¬ - p transistors to form ic. 0 b. None of these 4. 21. Sequential conspices are ostile to manipulate mathematical data. 1101 d. And doors are required to pass the tickets. a) Issuer ã ¢ â,¬: Logic high b) high threshold c) Integrated ¢ âgn saturated and not saturated and not saturated â € œ saturated libamils. DLD test questions and responses to practice libic design tests, lalic learning for schools and universities. 5. a) K.q b) K.q c) J.q d) J.q See answer: D Explanation: convert Mr. Flip to JK FLIP "FLOP" SR FLIP "SR entry SR Flop receives "J" and "Q" contributions through a door and a door. A priority encoder has four entries I0, I1, I2 and I3 where I3 has the highest priority and I0 has the minor minor a) 00 b) 01 c) 10 d) 11 View ATTENTION ATTENTION: C Explanation: In digital circuits, if an entry has 1, then the other entries with less priority can be considered with the condition of "Don". If i2 = 1, how will it be the exit? 39. a) Complete ¢ â,¬ - Summer b) undulating: transport carrier c) half â â,¬ - adder d) SUMMING VISION IN SERIES ANSWER: B Explanation: a â,¬ âgn Adder is a parallel binary summ) All of parity b) Check the whole of sum c) mã © all of generation of bits d) mã © all Odd-even view of response response: b Explanation: Check the sum enables to find double errors and also In finding the erroneous bits. What should be considered for a "care condition"? binary? a) act as a voltage source b) acts as a current sink c) acts as a current source d) acts as a voltage sink view: B Explanation: If the door exit is low in a circuit Digital TTL, the door must be able to sink the extracted current from the entrance of doors. a) 0 b) 1 c) either 0 or 1 d) Any number, except 0 and 1, see the response response: C Explanation: a care condition cannot take 0 or 1 according to the requirement. Infinite states 7. a) Combinational Lógic Circuits B) Sequential Lógic Circuits C) Both A and B D) None of the aforementioned views Answer: D Explanation: There are two main types of digital lógic circuits in digital electronic. a) 2 b) 4 c) 8 d) 16 Response view: d Explanation: In digital circuits, you can obtain a of 2n frequency of the pulsed clock signal connecting n flip "in the waterfall. The capacitance can be represented in terms of É¡rea and distance between the plates using the expressions c = aã®âµ0/d. The SOP expressions can consider it 1 for The number of expressions 1s and pos can consider that it is 0 to increase the number of 0s. As Amazon associate, I win the qualified purchases. A device that makes BCD seven segment is called A. Working sheets design MCQS digital libic, MÃ ºLTAS DLD options and answers for remote learning courses in line. 11. Then 1 kb = 210 B. 37. 26. What of the following is an example of a digital electronic? Inputs to a parallel circuit can be sent and processed at the same time unlike the serial circuits in which the inputs are sent one by one. According to the identity of the complementarity x + x = 1. You can practice these mcq chapter per capãtulo from the 1st chapter or can jump to any chapter of your choice. To perform the Boolean logic, digital circuits use transistors to generate liquid doors. 29. Fan: determines the number of entries that the private door can handle. 25. What will be the frequency of the output of a flip jk: flop, when j = 1, k = 1 and a pulse wave shape is given? What will be the output of a flip-flop d if d = 1 and the clock is low? 2. The established and restart pins NAND are high. The Truth Table of Mr. Flip, Flop and JK Flip are combined to obtain the expression. He lives in Bangalore and focuses on the development of Linux Kernel, San Technologies, Advanced C, Data Structures & Alongrithms. a) t b) 0 c) Clock d) 1 Response view: t Explanation: The entry in which the flip flop changes its condition when it synchronizes with the clock is called synchronous control inputs. 33. 14. Parallel admirers are used to add the partial products that are calculated using the doors and doors. a) 1 b) 2 c) 4 d) 8 Response response view: c Explanation: four 4 â,¬ ã ¢ â,¬ â € œBits binary binary together with 16 number of 2 â,¬: Contributions and doors to build a 4 bit: parallel multiplier. The high impedance at the exit will resist the conduct of many libic doors. While operating active active They help eliminate the turn, the delay of saturated transistors. After the analomic signals have been transformed digitally, the digital signal is applied. 3 â,¬ - Input and door are used, where 2 inputs come from each of the selection lines and 1 input for the data. It is said that ECL (emitter "coupled) and Schottky TTL are under the non -saturated logical family. The exit in a synchronic circuit depends on the mixture of entry signal present at that time and also of the past conditions of the past conditions . How many parallel binary admirers of 4 bits will be required to build a 4 -bit parallel multiplier? It is not determined by the past conditions. A) nand and nor b) and or c) nand and or d) and not see an answer To the explanation: the familiar family uses the Mosfet devices to perform their operation. The whole parity can help to find only individual errors within a word, since a double error will not change the bits of parity. The energy Ctric is provided in the circuit by a source of electricity, such as a batteria. DLD topics for summative and formative assessment are as: algorithmic state machinecomombinational logicssynchronous dryingus logicsstandard graphic symbolsasynchronous sequential LOGICBOOLEAN ALGEBRA AND LOGIC GATESBINARY SYSTEMSDLD LAB EQUIPMENT AND EXPERIMENTSSIMPLATION OF BOOAN FUNCTIONSMSI AND PLD COMPONENTS RUNNERS AND MEMORY MEMORY UNITSDIGITAL INTEGRATED CIRCITS CONCEPT: A DECODER WITH K INPUT LIES HAS 2K LESE A) torque b) quad c) Octeto d) Octave view Delivery: b Explanation: a group of 1s in 4 cells of a k ã ¢ â,¬ - map is called quad. a) When the clock is negative b) When the clock is positive c) When the tickets are all zero d) When the entries are all a view, answers, an explanation: a flip activated by negative level, the flop does not have a door present between the entrance of the clock and the entrance and the door. 2 b. They are: a) Combinational Lógic Circuits b) Sequential sequential Circuits 6. 24. 1011 b. A group of 1S in two cells is called a par and a group of 1S in four cells is a quad. Binary states 1111 at més high 6. What should be used together with synchronous control inputs to trigger a change in flip flop? 52. What determines the exit of the combinational liquid circuit in digital electronic? Therefore, for 4 flip ¢ â,¬: The frequency of the flip clock can be divided by 16. The result ã ¢ âgn These laws? The ECL family has a higher speed of change and dissipates more power. a) Past conditioning entry signals b) Boards of entry at the present time Future response Delivery: B Explanation: The exit in a combinational circuit depends on the entry mixture seals present at that time. a) XNOR Y XOR B) Y O C) O Y D) XOR AND XNOR VIEW RESPONSEWER: D Explanation: The xnor door is called a matching gate and gives 1 if there are similar entries similar to the door and the exit is 0 if different entries are given to the door. 17. Therefore, yz + xyz = (x + x) yz = yz. This oscillation between 0 and 1 leads to a race, around the condition that can be resolved using a teacher: Flip Slave Flop. What is a commutation function that has more than an exit called in digital electronics? It can be high or low depending on the relative magnitude of inputs 3. Keep connected to LinkedIn. Subscribe to your free master classes on YouTube and technical discussions in Telegram Sanfoundryclasses. a) four 2 âgn Explanation: four 4 â,¬ â,¬ â € 4 -bit parallel. A sequential code is a code in which each code of ã © xito is a binary number more than the previous code. What should be the entrance? entry? A "R" When Mr. Flip ": Flop becomes JK Flip"? 55. What of the following options are used in a current way: digital circuits? a) Less susceptible to noise or degradation in quality b) Use transistors to create liquid doors to perform the Boolean line View mentioned response of the update: D Explanation: a digital circuit is is a circuit that has a sign that must fall into one of two discrete levels. How many mistakes can the whole of the digital electronic parity in one word? What of the following is a type of digital libic circuit? a) Electronic field that involves the study of digital signal b) Engineering of devices that digital signal c) Engineering of devices that produce digital signal d) All view of the view mentioned response: D Explanation : Digital Electronics is a branch of electronics concerned with the study of digital seas, as well as the design design that use or generate them. The selection lines will help select a particular exit. 22. a) 8421 Code b) 2421 Code c) 5421 Code d) 2441 View of Códeigo Answer Answer: A EXPLANATION: A sequential cup . 5 states b. a) Two 16 x 1 mux b) three 8 x 1 mux c) two 8 x 1 mux d) three 16 x 1 mux view response: to explanation: two 16 x 1 mux will have given 32 entries. 15. A) PAR B) Quad c) Octet d) Octave View Delivery Answer: C Explanation: In a k ã ¢ â,¬ - Map: If there is a group of 1 in eight cells present, it makes an octet. a) Mãºltiple control b) Mistople of output c) more than an exit. What is the minimum distance required for the detection of enthusiasm in accordance with the Hamming Analysis in Digital Electronic? a) bass b) High capacitance c) Low inductance d) High inductance view Answer ATTENTION: A EXPLANATION: The TTL circuit uses transistors of a multiple emitter that have a small one. a) Lógica of the merged transistor b) Issuer ¢ â,¬ - Logic coupled c) Logic high threshold d) Resistance ã ¢ â,¬ - Logical view of the transistor response response: an explanation: inter ã ¢ â,¬: Integrated circuits may be represented by IIC or I2C are also called the transistor's libic fombug. What of the following provides the correct number of multiplexers necessary to build a 32 x 1 multiplexor? The digital libic design topics for distance learning courses are: Questions and answers from DLD questionnaires, objective DLD questions for CS career test preparation. How is the group of 1 present in 8 cells of a K map "? If you want How are the basic doors of the Mos Logic family? Therefore, 8421 is a sequential code. 5 Score: 0% range: Correct answer: here there are 1000 mcqs in digital circuits (chapter). 46. € It is one of the bit bit b) is a shock absorber c) It is a single bits inverter d) It is a view of the universal door response response: an explanation: ex â,¬, nor the door is a bits comparator of a bit comparator of a Only as the exit for the door is 1 if similar inputs are given to the door and the exit is 0 if different entries are given to the door. 10 ¢ £ â € "ã ¢ 210 decoders. a) Consensus Law b) Distributive Law c) Duality Law d) View of the Absorption Law Response D Explanation: The results 20. I2 = 1, therefore, i3 = 0, i1 = xy i0 = x. What contribution should be given to "is when Mr. Flip": flop becomes JK Flip "? It will be 10. a) When its output impedance is low and the input impedance is low b) When its output impedance is high and the input impedance is high c) When its output impedance is high and the input impedance It is low d) When the output impedance is low and the input impedance is high view of response: d Explanation: when the impedance of exit of a libic door is low and its impedance of entry is high, then a logical door It can conduct many other liquid doors. 41. I want the best in your effort to learn and master digital circuits! Manish Bhojasia, a veteran of technology with more than 20 years old @ cisco & wipro, is a founder and cto in Sanfoundry. Free MCQS with answers, preparation questions of competitive exits in line with digital libic design questionnaire with answers. The frequency of the output of a flip jk: flop, when j = 1, k = 1, and a pulse -shaped clock is given is half the clock input frequency. a) computers b) Information applications c) Digital cages d) All the view mentioned response response: D Explanation: Compute © Móviles, hard drives and computer memory The devices are examples of digital electronic. As the capacitance is directly proportional to the one, a small one leads to a lower capacitance. a) 2421 and 5211 b) 2421 and 8421 c) 5211 and 8421 d) 5421 and 2421 See answer: an explanation: a reflexive code is the one that the code for 9 is the complement of cóso for 0, the code for 8 is the Complement of Códeigo for 1, and so successively. Therefore, a flip activated by a negative level: the flop has a door not present between the clock entrance and the entrance and the door. 3 c. If they are due Double errors, you can use all verification: the sum can be used. used. used.

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